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FORM PTO-1390 (REV 10-94) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

DOCKET #: 4925-147PUS

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/937577

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FI00/00279	31 March 2000	01 April 1999

TITLE OF INVENTION

Method and arrangement for changing parallel clock signals in a digital data transmission

APPLICANT(S) FOR DO/EO/US

Harri LAHTI; Marko TORVINEN

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371
3. [x] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [x] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [x] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [x] has been transmitted by the International Bureau.
   c. [] is not required, as the application was filed in the United States Receiving Office (RO/US)
6. [] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [x] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C 371(c)(3))
   a. [] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [] have been transmitted by the International Bureau.
   c. [] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [x] have not been made and will not be made.
8. [] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). **Unexecuted**
10. [] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. Below concern other document(s) or information included:

11. [x] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [x] A **FIRST** preliminary amendment.
    [] A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. [] A substitute specification.
15. [] A change of power of attorney and/or address letter.
16. [x] Other items or information *(specify)*: PCT Publication Sheet, Int'l Preliminary Examination Report, Int'l Search Report, PCT Request, PCT Demand, Notice Informing the Applicant of the Communication of the International Application to the Designated Offices.

By Express Mail # EL895344575US

JC16 Rec'd PCT/PTO SEP 27 2001

U.S. APPLICATION NO (If known, see 37 C F R 1 5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/937577	PCT/FI00/00279	4925-147PUS

17.[x]The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO **$860.00**
International preliminary examination fee paid to USPTO (37 CFR 1.482)..... **$690.00**
No international preliminary examination fee paid to USPTO (37 CFR 1.482)
but international search fee paid to USPTO (37 CFR 1.445(a)(2))..... **$710.00**
Neither international preliminary examination fee (37 CFR 1.482)
nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$1000.00**
International preliminary examination fee paid to USPTO (37 CFR 1.482)
and all claims satisfied provisions of PCT Article 33(2)-(4) **$100.00**

			ENTER APPROPRIATE BASIC FEE AMOUNT =	$	860
Surcharge of **$130.00** for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$	
Claims	Number Filed	Number Extra	Rate		
Total Claims	12 - 20 =	0	x **$18.00**	$	0
Independent Claims	4 - 3 =	1	x **$80.00**	$	80
Multiple dependent claim(s) (if applicable)			+ **$270.00**	$	
			TOTAL OF ABOVE CALCULATIONS =	$	940
Reduction of ½ for filing by small entity, if applicable.				$	
			SUBTOTAL =	$	940
Processing fee of **$130.00** for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
			TOTAL NATIONAL FEE =	$	940
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by the appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
			TOTAL FEES ENCLOSED		$940
			Amount to be refunded:		$
			charged:		$

a. [x] One check in the amount of $ 940 to cover the above fees is enclosed.
b. [] Please charge my Deposit Account No. 03-2412 in the amount of $____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. [x] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 03-2412. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO
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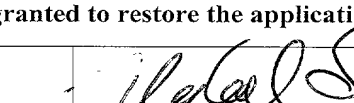

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Attorney Docket # 4925-147PUS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re National Phase PCT Application of

Harri LAHTI et al.

International Appln. No.: PCT/FI00/00279

International Filing Date: March 31, 2000

For: Method and arrangement for changing parallel clock signals in a digital data transmission

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231
BOX PCT

S I R:

Prior to examination of the above-identified application please amend the application as follows:

In the Claims:

Amend claim 5 to read as follows:

5. An indoor unit according to claim 3, characterised in that the indoor unit (31, 37) constitutes part of a radio link in a mobile telecommunications system.

Add the following new claim:

12. An indoor unit according to claim 4, characterised in that the indoor unit (31, 37) constitutes part of a radio link in a mobile telecommunications system.

REMARKS

This preliminary amendment is presented to place the application in proper form for examination and to eliminate multiple dependency from the present claims. No new matter has been added. Early examination and favorable consideration of the above-identified application is earnestly solicited.

Any additional fees or charges required at this time in connection with the application may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,
COHEN, PONTANI, LIEBERMAN & PAVANE

By: _____

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27 September 2001

AMENDMENTS TO CLAIMS

5. An indoor unit according to claim 3 [or 4], characterised in that the indoor unit (31, 37) constitutes part of a radio link in a mobile telecommunications system.

-Method and arrangement for changing parallel clock signals in a digital data transmission

The invention relates to a method and arrangement for changing parallel clock signals in the propagation assurance of digital data transmission, particularly for realising the propagation assurance of radio links. The invention is suited to other data transmission connections as well, for instance to connections using optical transmission paths.

The quality requirements for a digital radio link are generally known; said requirements are set for example by the ITU, International Telecommunication Union. The quality requirements refer to the reliability and interference-free quality of the transmission. The most important features are usability, error ratio and phase noise. Among the factors that affect the fulfilment of said criteria are hardware malfunctions, weather and changes in the signal path. In order to fulfil the requirements, it is necessary to provide an equipment and propagation assurance for the radio link, which means the use of alternative equipment and transmission paths. By means of equipment assurance, there is obtained a more reliable usability, and by propagation assurance, there is obtained both a lower error ratio and a lower phase noise.

Figure 1 is a block diagram illustrating one target of propagation assurance. A public switched telephone network (PSTN) 11 is connected by wires to a mobile switching centre (MSC) 12. The security of the radio link between the switching centre 12 and the base station controller (BSC) 13 is extremely important, wherefore it is generally assured. The controller 13 is further connected, by radio connections which can also be backed up, to base telecommunication stations (BTS) 14, 16, 18 and to their antennas 15, 17, 19.

The propagation assurance of radio links is realised by means of one or several parallel radio connections. Now in parallel with the major radio connection, there is constructed one or several other backup transmission paths that carry the same information. The transmission paths are preferably different in order to prevent possible interference caused by the terrain and/or weather changes from affecting both paths at the same time. Among the transmission paths, there is selected the one that has, in the prevailing conditions, a better signal at the station receiving the radio link. The applied criterion for the selection is generally the signal strength,

but also the correctness of the parity of the received information. The changing of the transmission path is carried out by means of a specific changeover device, in a way that is as error-free as possible, by compensating both the dynamic and static phase differences caused by the propagation of the signals in different transmission paths. The block dealing with the clock signal is the most critical part in the changeover device.

Among the drawbacks with known analog arrangements for changing the clock signal are the required separate components; in order to be able to use them, there is needed space on the circuit board and they consume a remarkable amount of power.

Another drawback with known analog arrangements is their cumbersome tuning as a final step in the production.

The object of the invention is to introduce an advanced method and arrangement for changing the clock signals in parallel transmission connections of a assured data transmission link. According to the method of the invention, the receiving transmission path is changed prior to losing the phase lock, and the data transmission of the link remains error-free, in case at least one of the transmission paths transmits the clock signal as sufficiently free of errors, even if errors should occur in another path.

This is realised so that through the parallel outdoor units (OU), located in succession to the common indoor unit (IU), there is sent a clock signal to the transmission paths, said clock signal is received by a second set of outdoor units, where the signal is locked by phase locked loops, and information of the mode of the phase lock is transmitted to the second indoor unit; further, there is chosen, in the receiving indoor unit, on the basis of the information obtained from the outdoor unit, a transmission path that contains less errors, in case errors occur with the employed connection. Here also a fading of the clock signal, leading to a disconnection from the phase lock, is considered as an error.

The invention relates to a method for changing parallel clock signals in digital data transmission. According to the invention, the changing of the clock signals is requested from the changeover device by a control signal based on a signal indicating an uncertainty in the locking, obtained from the phase locked loop; then there is expected a simultaneous signal pattern "11", i.e. an identical mode in order to get the signals in the same active part of the phase, as well as a turning in the

polarity of the signal phase difference, in order to obtain a situation where the signals have just recently been either in the same phase or in a phase shift of 180°, and after a delay DL, the clock signals are changed at a moment during which the clock signals in question are as near to phase coincidence as possible.

The invention relates to an indoor unit provided for digital data transmission and for changing the clock signal to be received among parallel clock signals of digital data transmission. According to the invention, the indoor unit includes an changeover device in order to receive and change a propagation assured clock signal on the basis of missing the locking.

The invention also relates to an outdoor unit provided for digital data transmission and for changing the parallel clock signals of digital data transmission. According to the invention, the outdoor unit includes a transmitter for transmitting the clock signal and respectively a receiver for receiving the clock signal, a phase lock synchronised with the received clock signal and further a signal output for indicating the mode of the synchronisation for the indoor unit.

The invention relates to an arrangement for changing parallel clock signals in digital data transmission, said arrangement comprising a first indoor unit for dividing the clock signals to be transmitted, antennas for transmitting and receiving parallel clock signals, and another indoor unit for selecting the clock signals to be received. According to the invention, it also comprises

- a first changeover device in the first indoor unit and a second changeover device in the second indoor unit in order to receive the propagation assured clock signal;

- in the transmission paths, a first and second outdoor unit in the transmitter transmitting the clock signal, and respectively in the receiver receiving the clock signal, as well as a phase lock which is synchronised with the received clock signal.

According to the invention, the changing of the transmission path is carried out always when the reception of the clock signal deteriorates to the extent that the loop that is phase locked to the clock signal does not keep in phase.

The changeover device can be realised with a fully application specific integrated circuit (ASIC).

An advantage of the invention is a shorter mean time between failure (MTBF) owing to a smaller number of components.

Preferred embodiments of the invention are set forth in the independent claims.

The invention is described in more detail below, with reference to the accompanying drawings, where

figure 1 is a block diagram illustrating a service environment according to the invention,

figure 2 is a flow diagram illustrating a method according to the invention,

figure 3 is a block diagram illustrating a link arrangement according to the invention,

figure 4 is a block diagram illustrating a known signal changeover device,

figure 5 is a block diagram illustrating a changeover device applying a clock signal multiplexer according to the invention,

figure 6 is a block diagram illustrating a clock signal multiplexer according to the invention,

figure 7 is a block diagram illustrating another clock signal multiplexer according to the invention, and

figure 8 is a block diagram illustrating a third clock signal multiplexer according to the invention.

Figure 1 was already dealt with above, in the description of the prior art.

The flow diagram of figure 2 illustrates the operation steps of a method according to the invention. The data flow to be transmitted is divided into two transmissions, and there is chosen a primary transmission path, i.e. a default path 21. The clock signal is transmitted, 22, through both transmission paths, for instance via a radio connection. When receiving the clock signals, the operational reliability of the loop that is phase locked to the clock signal is detected, 23, on both transmission paths. If the operational reliability of the phase locked loop is sufficient, the phase lock of the clock signal in the chosen transmission path is used, 26. If the operational reliability of the phase locked loop is not sufficient, 24, the chosen transmission path of the clock signal is changed, 25, by changing over to the phase lock which is

locked in the clock signal of the other transmission path. However, the clock signal is transmitted through both transmission paths.

Figure 3 is a block diagram illustrating the essential elements of a link arrangement according to the invention. An indoor unit (IU) 31 comprises a changeover device (CD) 32 for receiving propagation assured information. The first transmission path comprises an outdoor unit (OU) OU1 33, antennas 34, 35 and an outdoor unit OU1 36. On the right-hand side, there is shown an indoor unit IU 37 that is common for both transmission paths, and a changeover device CD 38 included in said indoor unit 37. The other transmission path comprises corresponding devices 39, 40, 41, 42. The selection of the transmission path for transmissions from left to right is carried out by the changeover device 38, and the selection of the transmission path for transmissions from right to left is carried out by the changeover device 32. The outdoor units 33, 36, 39, 42 comprise means 33A, 36A, 39A, 42A for creating and outputting the signal that indicates the mode of the synchronisation in the clock signal reception.

Figure 4 illustrates a prior art changeover device where the pairs of two clock signals CLK and a data signals DATA are changed. The elements outlined by the dotted line 41 are realised by an application specific integrated circuit (ASIC), and they include the following parts: an elastic buffer ELASTIC BUFFER 1 receiving the first signal pair CLK1, DATA1, an elastic buffer ELASTIC BUFFER 2 receiving the second signal pair CLK2, DATA2, a multiplexer REF MUX 44 of the reference clock signal, as well as a correlator and multiplexer CORR & MUX 47. Outside the integrated circuit, there are needed at least an analog low pass filter (LPF) 45 and a voltage controlled oscillator (VCO) 46. The difference in the write and read addresses of the active buffer 42 or 43 is conducted, via the multiplexer REF MUX 44, to the filter 45 in order to control the voltage controlled oscillator 46.

The writing to buffers is synchronised with incoming clock signals CLK1, CLK2, and the reading is synchronised by the output signal CLK of the voltage controlled oscillator 46, which signal is locked to the clock signal CLK1 or CLK2 of the active cable by the signal of the time difference between writing and reading the information, which signal is obtained from the buffer. The cable to be received is determined in the correlator 47, and there are created control signals CONTROL1, 2 for reading the buffers and a control signal CONTROL3 for controlling the multiplexer.

Figure 5 represents a block diagram of a signal changeover device according to the invention in an application specific integrated circuit. The clock signals CLK1, CLK2 of the received signal pairs are conducted to the clock signal multiplexer CLK MUX 51, where the clock signal to be received is selected. Both the clock signals CLK1, CLK2 and the data signals DATA1, 2 are also conducted to the data frame decoding blocks 52, 53, where the signals are used to create for example the following signals: synchronising signal SYNC, bit error signal (BE), frame alignment alarm signal (FAA), and pseudo frame signal (PF), as well as the data signals DATADF1, DATADF2 decoded from the frames. The outdoor unit OU activates the PF signal while loosing the locking of the clock signal CLK1, CLK2 to be received. In that case the data signal to be transmitted is replaced by a predetermined frame structure. The PF signal is used to indicate, prior to the FAA signal, an error situation in the reception of the clock signal CLK1, CLK2 in the indoor unit, and the FAA signal is only activated on the basis of several alignment errors in received frames. Owing to the pseudo frame structure, the data transmission between the outdoor unit OU and the indoor unit IU can be kept in operation even if the outdoor unit does not receive a proper clock signal. The signals are conducted to the blocks of elastic buffers EB & CTRL 54, 55, where also the selected clock signal CLK to be received is conducted in order to synchronise the data. From the blocks 54, 55, the data signals D1, D2 are conducted, by the data signal multiplexer DATA MUX 56, as a signal D to the decoding block 57. In the decoding block 57, the multiplexer 56 is controlled by the signal SYNC.

Figure 6 illustrates a clock signal multiplexer according to a preferred embodiment of the invention, which multiplexer waits for a suitable clock signal phase in order to change the signals, whereafter the signals are changed. The block 61 detecting the signal pattern "11" sends an active signal when the value of both clock signals CLK1, CLK2 is one. The D-flip-flop circuits 62, 63, 64 form a phase shift sensitive coupling, the outputs whereof are conducted to the block 65 detecting the signal patterns "01" and "10". Owing to said coupling, the output of the block 65 is raised to value one after a period of one clock cycle of the clock signal CLK2 has passed from the moment when the polarity of the phase difference between the clock signals CLK1, CLK2 was changed. Thus the phase difference at the moment of a rise in the output of the block 65 is virtually non-existent or 180°. If the signals are cophasal, they can be exchanged almost without a phase shift after a short delay DL 66. The changing of the clock signals by the multiplexer 68 is controlled by the block 67 checking the criteria of the changeover operation, which block 67 receives

as input signals a control signal requesting the changeover, a signal indicating the clock signal pattern "11" and a signal indicating the shift in the clock signal phase and delayed by the delay DL. On the basis of said criteria it is known that the signals are cophasal and not in a phase shift of 180°. The purpose of the delay DL is to ensure that the changing of the clock signals is carried out while the clock signals are, from the point of view of the system, in a static mode, i.e. in mode one. This prevents the creation of a disturbing voltage peak.

Figure 7 illustrates another clock signal changeover device according to the invention, which device comprises, in addition to the embodiment illustrated in figure 6, an analog phase-locked loop (APLL) 71 for synchronising the change, said loop multiplying the frequency of the second clock signal CLK2 by four. The output of the loop 71 is conducted to the block 67 that checks the changeover criteria. Owing to the use of the APLL, the delay DL illustrated in figure 6 is not needed here, because the changeover mode can be delayed by applying a later phase of the signal that was multiplied by four in frequency.

The block 61 indicating the clock signal pattern "11" can be realised for example by an AND gate. The block 65 indicating the pattern "01" or "10" can be realised for instance by an XOR gate. The block 86 indicating the pattern "10" can be realised for example by an inverter plus an AND gate.

Figure 8 illustrates a third clock signal changeover device according to the invention, wherein the phase difference between the signals is detected while the prevailing time difference is no longer than the delay DL. When the clock signal CLK1 is a little bit ahead of the clock signal CLK2, the output mode of the D-flip-flops 81, 82 is transmitted as one, but when the phase difference in any case causes a delay DL 83, the output mode of the D-flip-flops 84, 85 is transmitted as zero. Now the signals are considered to be sufficiently accurately cophasal, and the phase detector 86 obtains as input the output signals of the D-flip-flops 82, 85 in modes one and zero, and gives as output the signal one. The analog phase locked loop 71, the block 67 for checking the changeover criteria and the multiplexer 68 are otherwise operated in similar fashion as in the case of figures 6 and 7, but the block 67 only takes into account the loop 71, the phase detector 86 and the control signals.

The respective elements in the above described drawings 6, 7 and 8 are referred to by the same numbers in order to better illustrate the situation.

Let us now observe an example of a propagation assured radio link according to the invention, where the applied error correction method is an RS (63, 59) algorithm.

With both transmission paths in the outdoor units OU1, OU2, there is calculated a check sum for a data flow of the length of the period under observation, by multiplying the data RS (63, 59) to be checked by a primitive polynome. The check sum is added as a continuation to the data to be checked. Here the period of observation is 354 bits, i.e. 59 bytes, when one byte includes 6 bits. The length of the data frame formed by the payload information contained by said period plus the check sum is 378 bits, i.e. 63 bytes, of which the share of the check sum is 4 bytes.

Here the created data frames are transmitted via two different radio paths, which are susceptible to disturbances in ways that are as different as possible. Thus possible interference generally causes errors only in one transmission path at a time.

The received data frames are treated in receiving outdoor units OU1, OU2 by dividing the transmitted data frame by a generator polynome, so that a divisional remainder is obtained. The algorithm that locates errors uses said remainder for detecting errors. In addition to error detection, errors can also be corrected, in this case no more than two erroneous bytes. The maximum amount of bytes that can be corrected can be raised, by means of interleaving, up to eight bytes. The bytes are corrected, and there is calculated an error sum that indicates how many errors the received data contained. In the outdoor units OU1, OU2 there is created a data frame that contains the corrected payload information and the error sum.

The indoor unit IU receives from both outdoor units OU1, OU2 a data frame, and the changeover device CD selects, on the basis of the error sum, a better transmission path for the payload information to be further conducted to the output cable.

The invention can be used for example for backing up the links in radio networks conforming to the plesiochronous digital hierarchy (PDH). In that case, for instance the frequencies of radio links in the GSM network fluctuate within the range 7 - 38 GHz, and even a reading as high as 58 GHz is possible. In this type of application, the payload signal is a data signal of the plesiochronous digital hierarchy (PDH), with a general velocity of 2 Mbit/s or an even multiple thereof, but it may also be at least 34 Mbit/s. The length of the link is something between a hundred metres up to as much as several tens of kilometres.

Here an active mode of the signal means that the signal criteria are fulfilled. Thus the signal mode is true or advantageously one. The signal modes can also be inverted, in which case instead of mode "11", there is observed mode "00". The term 'identical modes' refers, however, to modes "11" or "00", and 'un-identical modes' means modes "01" or "10".

The indoor unit and outdoor unit here refer to the symbolic position of the unit in the system, and it does not restrict the location of said unit in the interior or exterior of a building.

Then number of transmission paths can be two or more.

The invention is not restricted to the above described embodiments only, but many modifications are possible within the scope of the inventive idea defined in the appended claims.

Claims

1. A method for changing parallel clock signals in a digital data transmission, **characterised** in that

- the changing of the clock signals is requested (25) from the changeover device by a control signal, based on a signal indicating the unreliability of the locking of the clock signal reception, said signal being received (23) from a phase locked loop.

- the system waits (25) until the clock signals were in the same, predetermined mode,

- the system waits (25) until the polarity of the signal phase difference is inverted, in order to reach a situation where the signals would have just been either in the same phase or in a phase shift of 180°, and

- after a delay DL, the clock signals are changed (25), in which case the changeover takes place at a moment which is as close to a phase coincidence of the clock signals to be changed as possible.

2. A method according to claim 1, **characterised** in that

- the changing of the clock signals is requested (25) by a control signal (CONTROL) from the changeover device, which control signal is based on a signal indicating an unreliability of the locking, said signal being received (23) from a phase locked loop,

- in the block that detects identical modes of the clock signals, there is transmitted (25) a detection signal, when both clock signals (CLK1, CLK2) are in the same mode,

- there is formed (25), by a phase shift sensitive coupling, for the block that detects un-identical modes of the clock signals, a signal for indicating a change in the polarity of the phase difference,

- there is transmitted (25), in a delayed fashion, a signal indicating the change in the polarity of the phase difference for the block checking that the criteria for realising the changeover are fulfilled, when it is detected that the clock signals are in different modes,

- the multiplexer is regulated (25) to change the clock signals, when at least the control signal (CONTROL), the signal detecting identical modes of the clock signals and the signal indicating a change in the polarity of the phase difference to be delayed are active, to the mode indicated by the control signal (CONTROL).

3. An indoor unit (31, 37) for digital data transmission and for changing parallel clock signals in digital data transmission, **characterised** in that the indoor unit comprises a changeover device (38) for receiving and changing the clock signal on the basis of missing the locking of the clock signal reception.

4. An indoor unit according to claim 3, **characterised** in that the changeover device (38) is realised in an application specific integrated circuit and comprises

- a clock signal multiplexer (51) for selecting the clock signals (CLK1, CLK2) for the signal pairs to be received as the clock signal (CLK) to be received, by waiting for a suitable clock signal phase in order to change said signals and by then performing the changeover,

- at least two data frame decoding blocks (52, 53) where the clock signals (CLK1, CLK2) and the data signals (DATA1, DATA2) are formed into control signals and data signals (DATADF1, DATADF2) decoded from the frames,

- at least two elastic buffer and control blocks (54, 55) where by means of control signals and decoded data signals (DATADF1, DATADF2), there are formed data signals (D1, D2) that are synchronised by the clock signal (CLK) to be received,

- a data signal multiplexer (56) for selecting the data signal (D) to be received, by regulating by the control signal (SYNC), and

- a decoding block (57) in order to synchronise the received data signal (D) by means of the received clock signal (CLK) into a final data signal (DATA) and for controlling the data signal multiplexer (56) by means of the control signal (SYNC).

5. An indoor unit according to claim 3 or 4, **characterised** in that the indoor unit (31, 37) constitutes part of a radio link in a mobile telecommunications system.

6. An outdoor unit (33, 36) for digital data transmission and for changing parallel clock signals in digital data transmission, **characterised** in that said outdoor unit comprises a transmitter for transmitting the clock signal to be changed and respectively a receiver for receiving said clock signal, and a phase lock to be

synchronised with the received clock signal and further means (33A, 36A) for outputting a signal that indicates the mode of the synchronisation.

7. An outdoor unit according to claim 6, **characterised** in that the outdoor unit is part of a radio link in a mobile telecommunications system.

8. An arrangement for changing parallel clock signals in digital data transmission, said arrangement comprising a first indoor unit (31) for dividing the clock signals to be transmitted, antennas (34, 35, 40, 41) for transmitting and receiving parallel clock signals and a second indoor unit (37) for selecting the clock signals to be received, **characterised** in that said arrangement also comprises

- a first changeover device (32) in the first indoor unit (31) and a second changeover device (38) in the second indoor unit (37) for receiving the propagation assured clock signal, and

- a first (33) and second outdoor unit (36) provided with a transmitter for transmitting the clock signal to be changed and respectively a receiver for receiving the clock signal, and a phase lock synchronised with the received clock signal.

9. An arrangement according to claim 8, **characterised** in that the changeover device (38) is realised in an application specific integrated circuit and comprises

- a clock signal multiplexer (51) for selecting the clock signals (CLK1, CLK2) of the signal pairs to be received as the clock signal (CLK) to be received, by waiting for a suitable phase of the clock signals in order to change said signals and by performing the changeover,

- at least two data frame decoding blocks (52, 53), wherein of the clock signals (CLK1, CLK2) and of the data signals (DATA1, DATA2) there are formed the control signals and data signals (DATADF1, DATADF2) decoded from the frames,

- at least two elastic buffer and control blocks (54, 55), wherein by means of the control signals and decoded data signals (DATADF1, DATADF2), there are formed the data signals (D1, D2) to be synchronised by the clock signal (CLK) to be received,

- a data signal multiplexer (56) for selecting the data signal (D) to be received by controlling with the control signal (SYNC), and

- a decoding block (57) for synchronising the received data signal (D) by means of the received clock signal (CLK) as the final data signal (DATA) and for controlling the data signal multiplexer (56) by a control signal (SYNC).

10. An arrangement according to claim 9, **characterised** in that the control signals include the following signals: a synchronising signal SYNC, a bit error signal BE, a frame alignment alarm signal FAA and a pseudo frame signal PF.

11. An arrangement according to claim 9, **characterised** in that the clock signal multiplexer (51) comprises

- a block (61) for detecting un-identical modes of the clock signals, which block gives an active signal when both clock signals CLK1, CLK2 are in the same mode,

- D-flip-flop circuits (62, 63, 64), which form a phase shift sensitive coupling,

- a block (65) for detecting un-identical modes of the clock signals, whereto there are conducted the outputs from the phase shift sensitive coupling, and the output of said block (65) is raised, owing to said coupling, to the value one after a period of one cycle of the second clock signal CLK2 has passed from the moment when the polarity of the phase difference between the clock signals CLK1, CLK2 was changed,

- a delay circuit (66) for delaying the output signal from the block (65) that detects un-identical modes of the clock signals,

- a block (67) for checking the criteria for the clock signal changeover, in order to check the mode of the changeover request control signal, the output signal from the block (61) detecting identical modes of the clock signals, and the output signal from the delay block (66), and

- a multiplexer (68) for performing the clock signal changeover under the control of the block (67) that checks the criteria, when the phase difference between the clock signals is virtually non-existent.

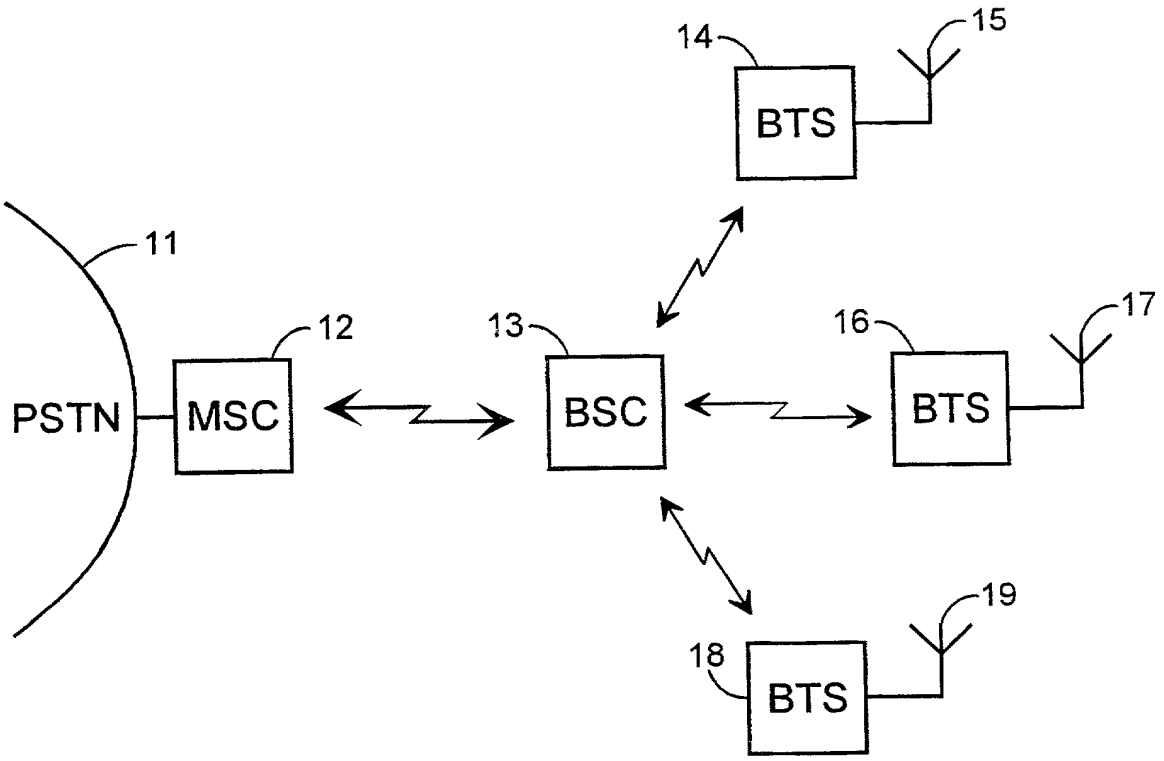

FIG. 1

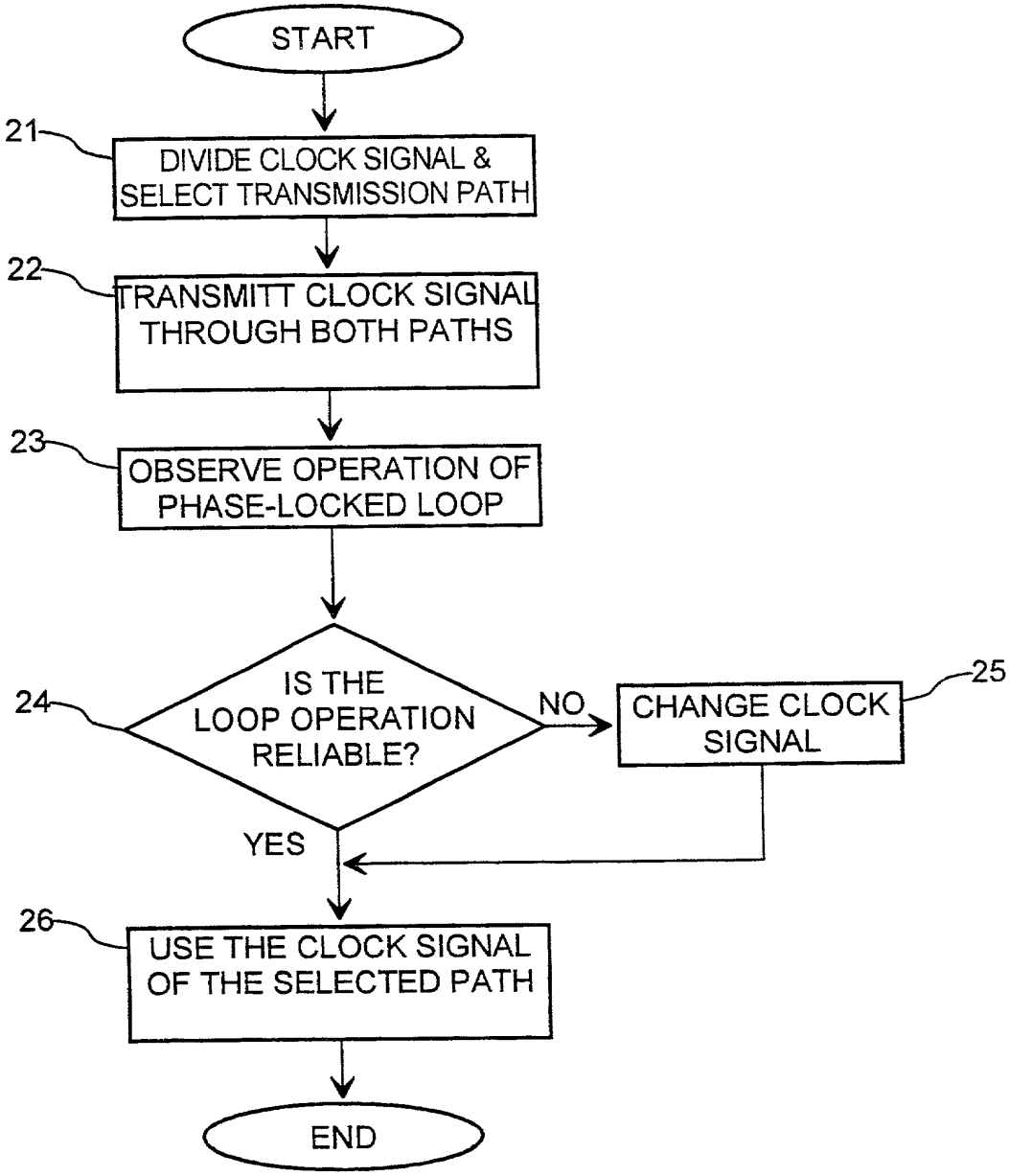

FIG. 2

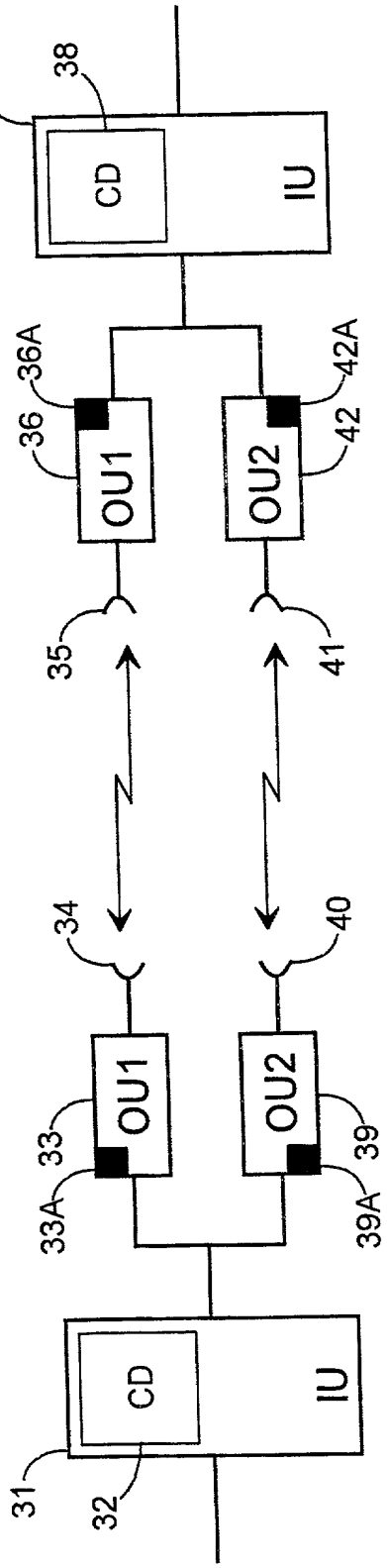
37
38
CD
IU
36A
36
OU1
42A
42
OU2
35
41
34
40
33
OU1
OU2
39
33A
39A
CD
IU
31
32

FIG. 3

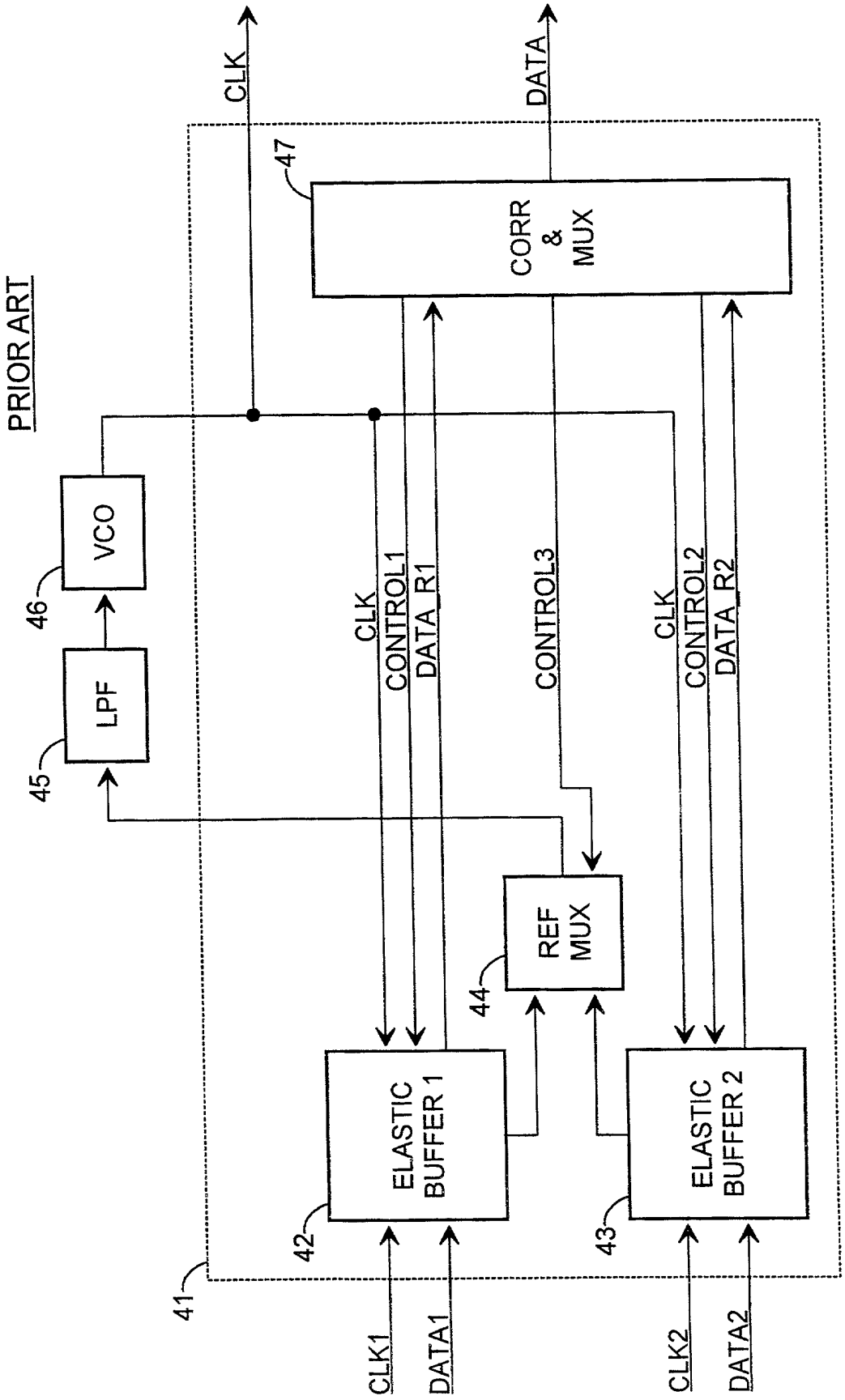

FIG. 4

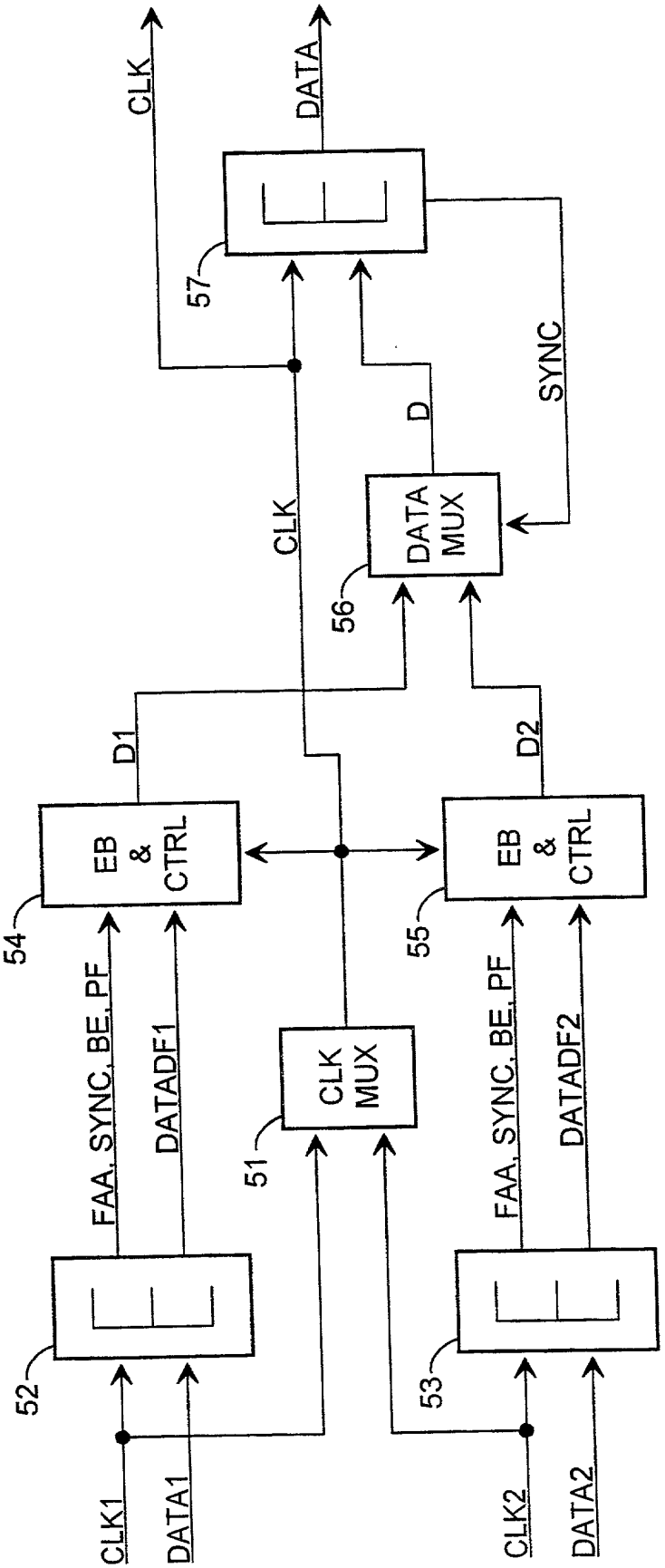
CLK
DATA
57
SYNC
D
CLK
DATA MUX
56
D1
D2
EB & CTRL
54
EB & CTRL
55
FAA, SYNC, BE, PF
DATADF1
FAA, SYNC, BE, PF
DATADF2
CLK MUX
51
52
53
CLK1
DATA1
CLK2
DATA2

FIG. 5

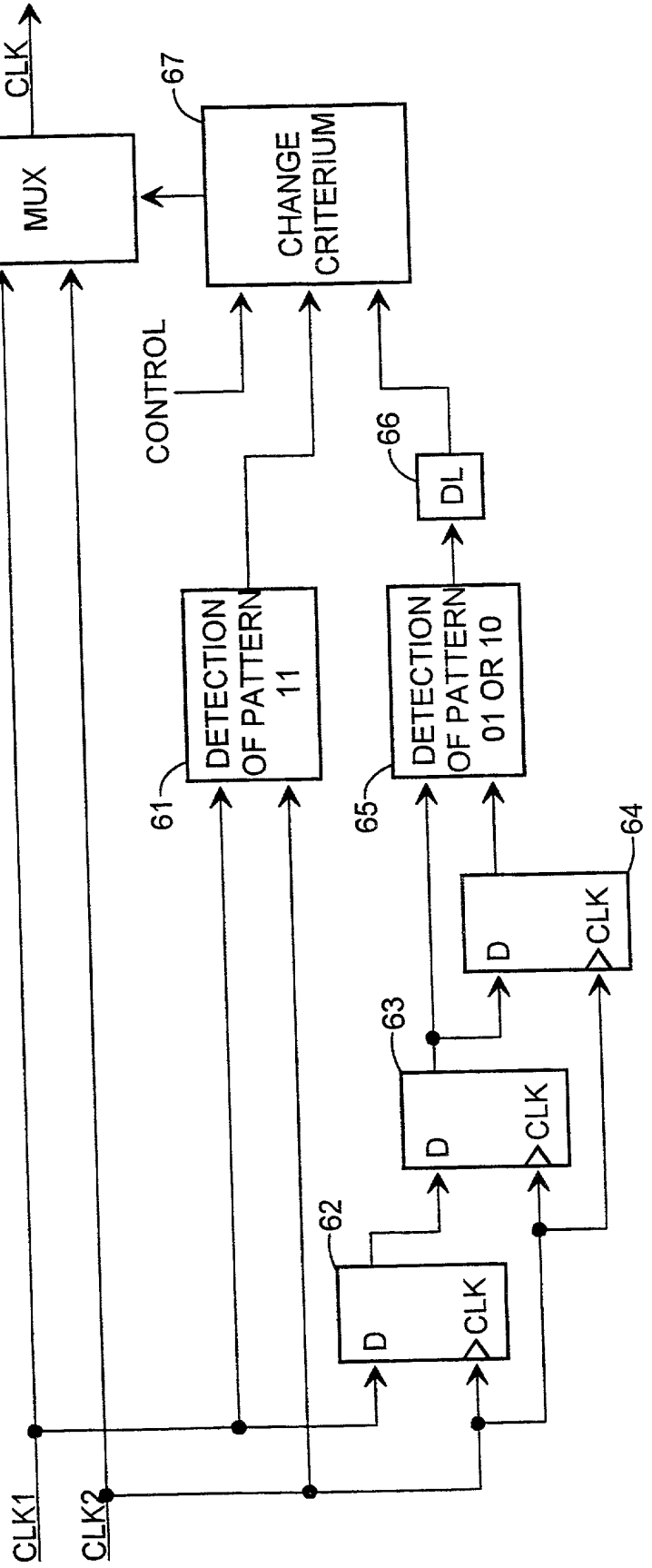
CLK
68
MUX
67
CHANGE CRITERIUM
CONTROL
66
DL
DETECTION OF PATTERN 11
61
DETECTION OF PATTERN 01 OR 10
65
64
D
CLK
63
62
CLK1
CLK2

FIG. 6

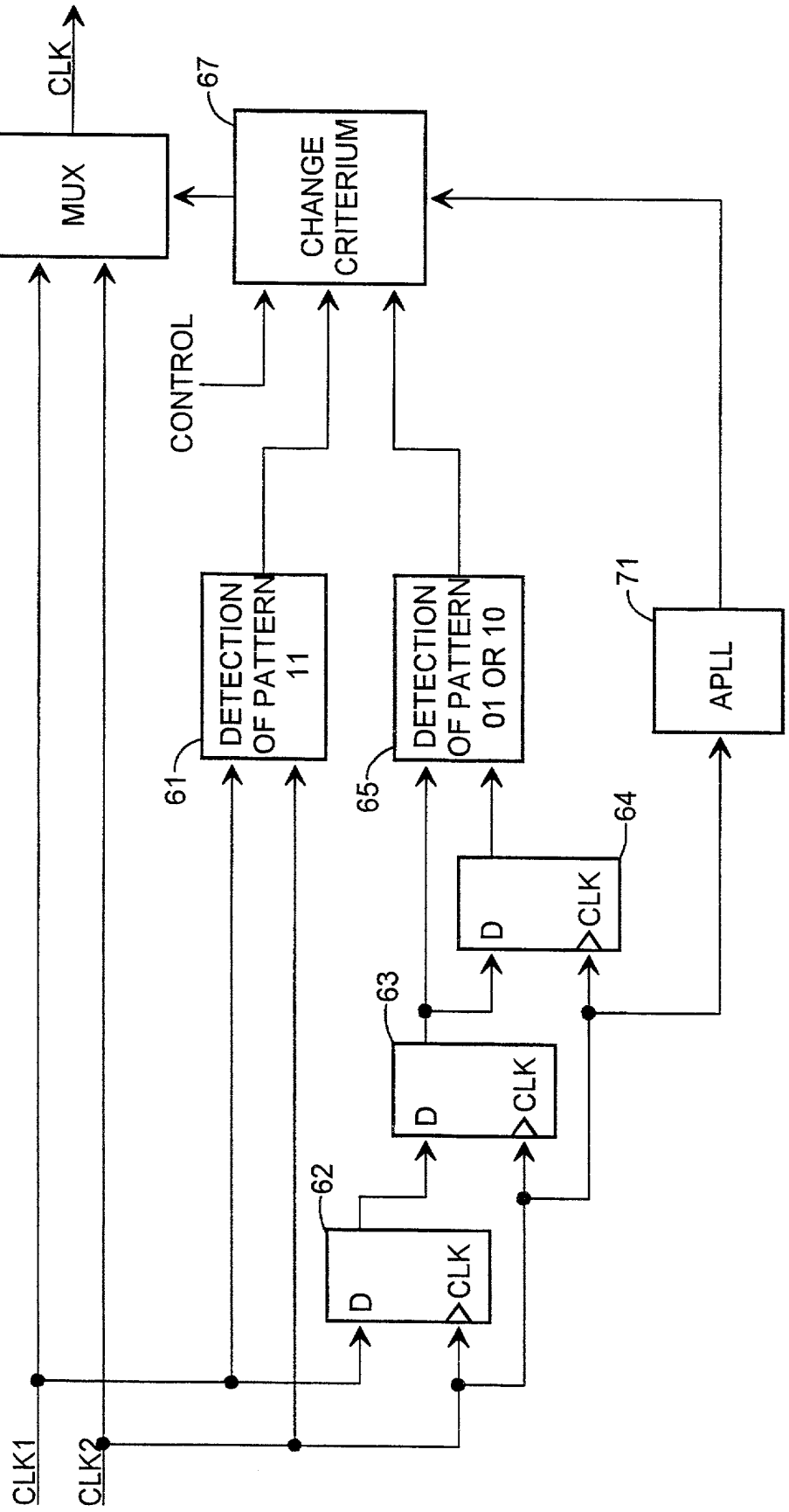

FIG. 7

09/937577

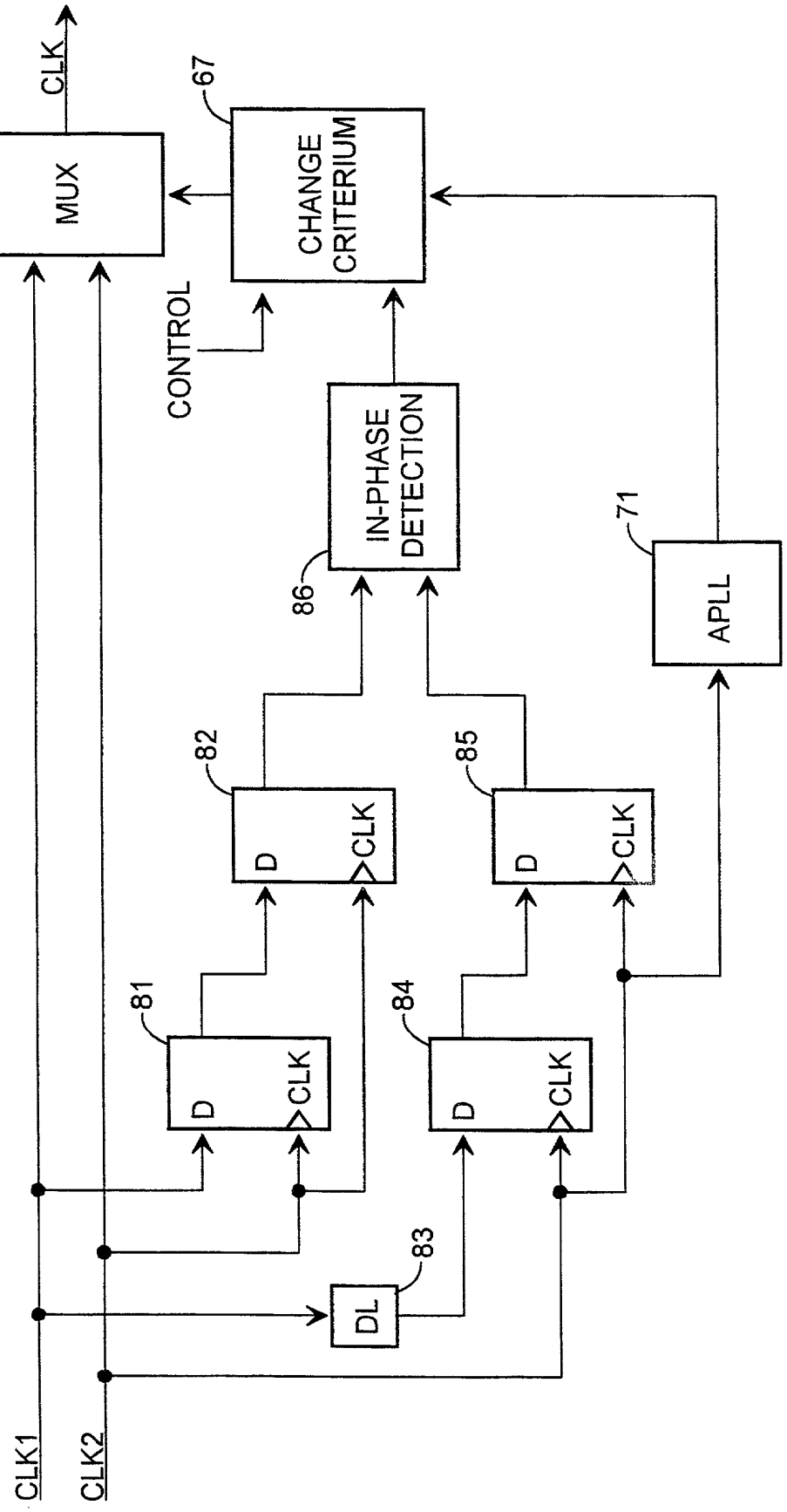

FIG. 8

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY Includes Reference to PCT International Applications	Attorney's Docket No 4925-147PUS

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND ARRANGEMENT FOR CHANGING PARALLEL CLOCK SIGNALS IN A DIGITAL DATA TRANSMISSION

the specification of which (check only one item below)

[] is attached hereto

[] was filed as United States application

Serial No. _

on _

and was amended

on _ (if applicable).

[x] was filed as PCT international application

Number PCT/FI00/00279

on 31 March 2000

and was amended under PCT Article 19

on _ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

PRIOR FOREIGN/PCT APPLICATIONS AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

Country (if PCT, indicate "PCT")	Application Number	Date of Filing (day, month, year)	Priority Claimed Under 35 U.S.C. 119	
Finland	990738	01 April 1999	[x] YES	[] NO
PCT	PCT/FI00/00279	31 March 2000	[x] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO

Combined Declaration for Patent Application and Power of Attorney (Continued) (Includes Reference to PCT International Applications)	Attorney's Docket No 4925-147PUS

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1 56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS *(check one)*		
U.S APPLICATION NUMBER	U S FILING DATE	PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO. / PCT FILING DATE / U S SERIAL NUMBERS ASSIGNED *(if any)*				
PCT/FI00/00279	31 March 2000		X	

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*List name and registration number*)

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Combined Declaration for Patent Application and Power of Attorney (Continued) (Includes Reference to PCT International Applications)				Attorney's Docket No. 4925-147PUS
203	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE 11/02/2001	DATE 11/06/2001	DATE